|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Symbol** | **Parameter** | **Condition** | **Minimum** | **Typical** | **Maximum** | **Unit** |
| **Input DC Specifications** | | | | | | |
| VI | Input signal voltage range |  | -50 |  | 1350 | mv |
| ILEAK | Input leakage current | Note1 | -10 |  | 10 | μA |
| VGNDSH | Ground shift |  | -50 |  | 50 | mv |
| VOH(absmax) | Maximum transient output voltage level |  | -0.15 |  | 1.45 | v |
| tVOH(absmax) | Maximum transient time above VOH(absmax) |  |  |  | 20 | ns |
| **HS Line Drivers DC Specifications** | | | | | | |
| |VOD| | HS Transmit Differential output voltage magnitude | Note2 | 140 | 200 | 270 | mv |
| Δ|VOD| | Change in Differential output voltage magnitude between logic states | Note2 |  |  | 14 | mv |
| VCMTX | Steady-state  common-mode output  voltage | Note2 | 150 | 200 | 250 | mv |
| ΔVCMTX(1,0) | Changes in steady-state common-mode output voltage between logic states | Note2 |  |  | 5 | mv |
| VOHHS | HS output high voltage | Note2 |  |  | 360 | mv |
| ZOS | Single-ended output impedance |  | 40 | 50 | 62.5 | Ω |
| ΔZOS | Single-ended output  impedance mismatch |  |  |  | 10 | % |
| NOTE |  | | | | | |
| **LP Line Drivers DC Specifications** | | | | | | |
| VOL | Output low-level SE voltage |  | -50 |  | 50 | mv |
| VOH | Output high-level SE voltage |  | 1.1 | 1.2 | 1.3 | v |
| ZOLP | Single-ended output impedance |  | 110 |  |  | Ω |
| ΔZOLP(01,10) | Single-ended output impedance mismatch driving opposite level |  |  |  | 20 | % |
| ΔZOLP(00,11) | Single-ended output impedance mismatch driving same level |  |  |  | 5 | % |
| **HS Line Receiver DC Specifications** | | | | | | |
| VIDTH | Differential input high voltage threshold |  |  |  | 70 | mv |
| VIDTL | Differential input low voltage threshold |  | -70 |  |  | mv |
| VIHHS | Single ended input high voltage |  |  |  | 460 | mv |
| VILHS | Single ended input low voltage |  | -40 |  |  | mv |
| VCMRXDC | Input common mode voltage |  | 70 |  | 330 | mv |
| ZID | Differential input impedance |  | 80 |  | 125 | Ω |
| **LP Line Receiver DC Specifications** | | | | | | |
| VIL | Input low voltage |  |  |  | 550 | mv |
| VIh | Input high voltage |  | 880 |  |  | mv |
| VHYST | Input hysteresis |  | 25 |  |  | mv |
| **Contention Line Receiver DC Specifications** | | | | | | |
| VILF | Input low fault threshold |  |  |  | 200 | mv |
| VIHF | Input high fault threshold |  | 450 |  |  | mv |
| **HS Line Drivers AC Specifications** | | | | | | |
| FDDRCLK | DDR CLK frequency | On CLKP/N outputs | 40 |  | 750 | MHz |
| UIINST | UI instantaneous | Note3 |  |  | 12.5 | ns |
| ΔUI | UI variation | Note4 | -10% |  | 10% | UI |
| Note5 | -5% |  | 5% | UI |
| tCDC | DDR CLK duty cycle | tCDC=tCPH/PDDRCLK |  | 50 |  | % |
| tCPH | DDR CLK high time |  |  | 1 |  | UI |
| tCPL | DDR CLK low time |  |  | 1 |  | UI |
| - | DDR CLK / DATA Jitter | Note6 |  | 75 |  | ps pk-pk |
| tSKEW[PN] | Intra-Pair (Pulse) skew |  |  | 0.075 |  | UI |
| tSKEW[TX] | Data to Clock Skew | Note7 | -0.15 |  | 0.15 | UI |
| Note8 | -0.20 |  | 0.20 | UI |
| tSETUP[RX] | Data to Clock Receiver Setup time | Note9 | 0.15 |  |  | UI |
| Note10 | 0.20 |  |  | UI |
| tHOLD[RX] | Clock to Data Receiver Hold time | Note9 | 0.15 |  |  | UI |
| Note10 | 0.20 |  |  | UI |
| tr | Differential output signal rise time | 20% to 80%, RL = 50Ω, Note11 |  |  | 0.30 | UI |
| 20% to 80%, RL = 50Ω, Note12 |  |  | 0.35 | UI |
| 20% to 80%, RL = 50Ω, Note13 | 100 |  |  | ps |
| tf | Differential output signal fall time | 20% to 80%, RL = 50Ω, Note11 |  |  | 0.30 | UI |
| 20% to 80%, RL = 50Ω, Note12 |  |  | 0.35 | UI |
| 20% to 80%, RL = 50Ω, Note13 | 100 |  |  | ps |
| ΔVCMTX(HF) | Common level variation above 450 MHz | 80Ω≤RL≤125Ω |  |  | 15 | mVrms |
| ΔVCMTX(LF) | Common level variation between 50 MHz and 450 MHz | 80Ω≤RL≤125Ω |  |  | 25 | mVp |
| **LP Line Drivers AC Specifications** | | | | | | |
| trlp , tflp | Single ended output rise/fall time | 15% to 85%, CL < 70 pF |  |  | 25 | ns |
| treot |  | 30% to 85%, CL < 70 pF |  |  | 35 | ns |
| ∂V/∂tSR | Signal slew rate | 15% to 85%, CL < 70 pF,Note14 |  |  | 150 | mV/ns |
| CL | Load capacitance | Note15 | 0 |  | 70 | pF |
| **HS Line Receiver AC Specifications** | | | | | | |
| ΔVCMRX(HF) | Common mode interference beyond 450 MHz |  |  |  | 200 | mVpp |
| ΔVCMRX(LF) | Common mode interference between 50 MHz and 450 MHz |  | -50 |  | 50 | mVpp |
| CCM | Common mode termination | Note16 |  |  | 60 | pF |
| **LP Line Receiver AC Specifications** | | | | | | |
| eSPIKE | Input pulse rejection |  |  |  | 300 | V.ps |
| TMIN | Minimum pulse response |  | 20 |  |  | ns |
| VINT | Pk-to-Pk interference voltage |  |  |  | 400 | mVpp |
| fINT | Interference frequency |  | 450 |  |  | MHZ |
| **Note** | 1. VGNDSH(min) ≤ VI ≤ VGNDSH(max) + VOH(absmax) . Lane module in LP receive mode.  2. 80Ω≤RL≤125Ω  3. This value corresponds to a minimum Mbps data rate.  4. When UI ≥ 1ns, within a single burst.  5. When UI < 1ns, within a single burst.  6. Jitter specification with clean clock at REFCLK input.  7. Total silicon and package skew delay budget of 0.3\*UIINST when D-PHY is supporting maximum data rate = 1 Gbps.  8. Total silicon and package skew delay budget of 0.4\* UIINST when D-PHY is supporting maximum data rate > 1 Gbps.  9. Total setup and hold window for receiver of 0.3\* UIINST when D-PHY is supporting maximum data rate = 1 Gbps.  10. Total setup and hold window for receiver of 0.4\* UIINST when D-PHY is supporting maximum data rate > 1 Gbps.  11. Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).  12. Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).  13. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.  14. Measured as average across any 50 mV of the output signal transition.  15. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.  16. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification. | | | | | |